**Lab report no 11**



**Fall 2021**

# Computer Architecture and organization Lab

**Submitted By**

**Names Registration No**

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Section: **A**

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**Task no 1 (2x1): -**

**Code: -**

**Mux2x1: -**

module mux2x1(A,B,set,f);

input A,B,set;

output f;

wire nset,f1,f2;

not n1(nset,set);

and a1(f1,A,nset);

and a2(f2,B,set);

or o1(f,f1,f2);

endmodule

module stim();

reg A,B,set;

wire f;

mux2x1 t(A,B,set,f);

initial

begin

$display ("A B set f");

A=0;B=0; set=0;

#10 $display("%b %b %b %b",A,B,set,f);

A=0;B=0; set=1;

#10 $display("%b %b %b %b",A,B,set,f);

A=0;B=1; set=0;

#10 $display("%b %b %b %b",A,B,set,f);

A=0;B=1; set=1;

#10 $display("%b %b %b %b",A,B,set,f);

A=1;B=0; set=0;

#10 $display("%b %b %b %b",A,B,set,f);

A=0;B=1; set=1;

#10 $display("%b %b %b %b",A,B,set,f);

A=0;B=0; set=1;

#10 $display("%b %b %b %b",A,B,set,f);

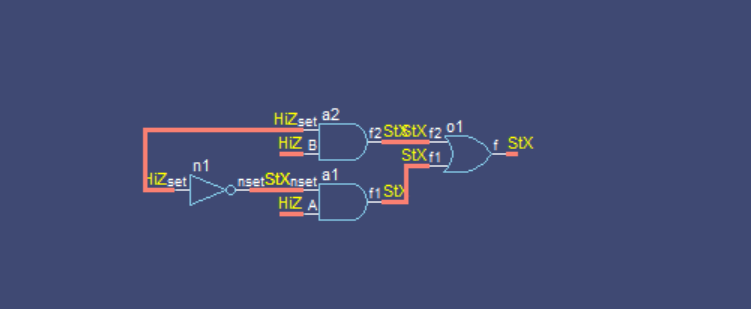
A=1;B=1; set=1;

#10 $display("%b %b %b %b",A,B,set,f);

end

endmodule

**Design circuit: -**



**Task no 2 : -**

**Mux4x1: -**

module mux4x1(A,B,C,D,set0,set1,f);

input A,B,C,D,set0,set1;

output f;

wire nset0,nset1,f1,f2,f3,f4;

not n1(nset0,nset1,set0,set1);

and a1(f1,nset1,A,nset0);

and a2(f2,nset1,B,set0);

and a3(f3,set1,C,nset0);

and a4(f4,set1,D,set0);

or o1(f,f1,f2,f3,f4);

endmodule

module stim();

reg A,B,C,D,set0,set1;

wire f;

mux4x1 t(A,B,C,D,set0,set1,f);

initial

begin

$display ("A B C D set0 set1 f");

A=0; B=0; C=0; D=0;set0=0; set1=0;

#10 $display("%b %b %b %b %b %b %b",A,B,C,D,set0,set1,f);

A=0;B=0; C=0; D=0; set0=0; set1=1;

#10 $display("%b %b %b %b %b %b %b",A,B,C,D,set0,set1,f);

A=0;B=0; C=0; D=1; set0=0; set1=1;

#10 $display("%b %b %b %b %b %b %b",A,B,C,D,set0,set1,f);

A=0;B=0; C=1; D=0; set0=0; set1=1;

#10 $display("%b %b %b %b %b %b %b",A,B,C,D,set0,set1,f);

A=0;B=1; C=0; D=0; set0=0; set1=1;

#10 $display("%b %b %b %b %b %b %b",A,B,C,D,set0,set1,f);

A=1;B=0; C=0; D=0; set0=0; set1=1;

#10 $display("%b %b %b %b %b %b %b",A,B,C,D,set0,set1,f);

A=0;B=0; C=1; D=1; set0=0; set1=1;

#10 $display("%b %b %b %b %b %b %b",A,B,C,D,set0,set1,f);

A=0;B=1; C=0; D=1; set0=0; set1=1;

#10 $display("%b %b %b %b %b %b %b",A,B,C,D,set0,set1,f);

A=0;B=0; C=1; D=0; set0=0; set1=1;

#10 $display("%b %b %b %b %b %b %b",A,B,C,D,set0,set1,f);

A=0;B=1; C=1; D=0; set0=0; set1=1;

#10 $display("%b %b %b %b %b %b %b",A,B,C,D,set0,set1,f);

A=1;B=0; C=0; D=1; set0=0; set1=1;

#10 $display("%b %b %b %b %b %b %b",A,B,C,D,set0,set1,f);

A=1;B=0; C=1; D=1; set0=0; set1=1;

#10 $display("%b %b %b %b %b %b %b",A,B,C,D,set0,set1,f);

A=1;B=1; C=0; D=1; set0=0; set1=1;

#10 $display("%b %b %b %b %b %b %b",A,B,C,D,set0,set1,f);

A=1;B=1; C=1; D=0; set0=0; set1=1;

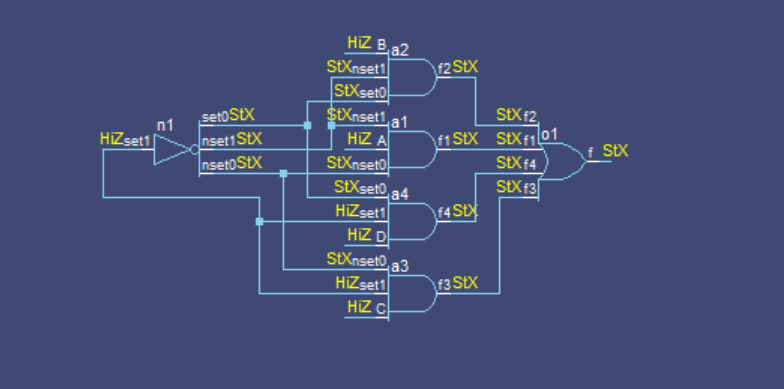
#10 $display("%b %b %b %b %b %b %b",A,B,C,D,set0,set1,f);

A=1;B=1; C=1; D=1; set0=0; set1=1;

end

endmodule

**Design circuit: -**



**Task no 2 (Half adder): -**

**Code: -**

**Half adder module: -**

module halfadder(A,B,f1,f2);

input A,B;

output f1,f2;

and a1(f1,A,B);

xor a2(f2,A,B);

endmodule

**Stim: -**

module stim();

reg A,B;

wire f1,f2;

halfadder t(A,B,f1,f2);

initial

begin

$display ("A B f1 f2");

A=0;B=0;

#10 $display("%b %b %b %b",A,B,f1,f2);

A=0;B=1;

#10 $display("%b %b %b %b",A,B,f1,f2);

A=1;B=0;

#10 $display("%b %b %b %b",A,B,f1,f2);

A=1;B=1;

#10 $display("%b %b %b %b",A,B,f1,f2);

end

endmodule

**Design circuit: -**

